PCB Co-Design Layout Engineer

The candidate will work in a team oriented environment to perform PCB layout and related tasks as a key part of chip, package, and PCB co-design for ASIC development systems and products. This engineer must interface with system & board designers, packaging engineers, reference platform design teams, and signal integrity engineers to guide them on board routing tradeoffs for given design rules and signal and power integrity constraints. Working effectively across organizational boundaries is essential as is the effective communication and documentation of results. The candidate must be able to work effectively with incomplete or vaguely defined requirements and to support multiple projects at once while dealing with frequent priority and constraint changes.

Responsibilities:

- Work with system engineers to understand design objectives and constraints, document deliverables, and implement deliverables
- Develop and maintain accuracy of task duration and schedule estimates for defined deliverables for multiple simultaneously active projects
- Perform PCB database configurations including stack-up and design rule integration
- Perform layout assessments for high density ASIC using PCB stack-up and design rules consistent with targeted markets. This will include:
    * Component placement and optimization
    * Signal breakout and routing analysis
    * Power domain breakout and routing analysis
    * Memory, serial, RF, and other IO detailed complete routing implementation
    * Provide data to drive necessary changes in stack-up, design rules, and constraints
    * Iteratively provide feedback to package and chip designers to improve designs
- Work with system engineers and signal and power integrity engineers to facilitate iterative electrical analysis (e.g., model extraction, frequency and time domain simulations) to support system co-design.
- Work with downstream groups to leverage layout results for design guidance or direct copying of design portions.

Skills/Experience:

Targeted Skills/Experience:

- Competency with Mentor Expedition or Cadence Allegro board design flows, including constraint and design rule configuration, layout, and design fabrication preparation
- Strong oral and written communication skills, including fluency in written and spoken American English

Additional Applicable Skills:

- Experience with Cadence SiP
- Experience with VBscript, Perl, or Skill
- Familiarity with basic signal or power integrity concepts

Education:

Minimum of Associate degree in EE Technology or related discipline or equivalent experience; at least 3 years of relevant commercial experience.

How to Apply:

Qualified candidates should respond to Julia Katawazi at jkatawazi@coleman.edu by submitting your **resume**. Include Front-End Specialist in the email subject line.